Sub Code: ECT033 **ROLL NO……..……..**

EVEN SEMESTER EXAMINATION, 2023 – 24

2ND yr B.Tech. – CS&E/AI&ML

DIGITAL ELECTRONICS

Duration: 3:00 hrs **Max Marks: 100**

Note: - Attempt all questions. All Questions carry equal marks. In case of any ambiguity or missing data, the same may be assumed and state the assumption made in the answer.

Q 1.	Answer any four parts of the following. a) Define the term universal gates and their applications. Define the term universal gates and their applications. b) Convert the following, 1. (5162)10 = ()2 2. (11011001)2 = ()10 3. (6273)10 = ()8 4. (7860)10 = ()16 5. (A23B8)16 = ()10 c) What are the VHDL constructs used for combinational circuits and sequential circuits? d) Using active high output 3:8 line decoder, implement the following functions F1(A, B, C, D) =Σ m (0,1,2,5,7,11,15) F2(A, B, C, D) =Π m (1,3,4,11,13,14) e) Define the TTL (Transistor-Transistor-Logic) logic Family used for digital circuits. f) Define the De-morgan's theorem of Logic Simplification for SOP & POS forms.	5x4=20
Q 2.	Answer any four parts of the following. a) Elaborate the characteristic equations of S-R and J-K Flip-Flops. b) Explain difference between latch and flip-flop. c) What are the differences between Combinational Circuits and Sequential Circuits? Convert the Gray Code 111001 into binary code. d) What is race around condition in JK flip-flop? Find the 'x' base of (211)x=(152)8? e) Define the following term in digital circuits? i) Noise Margin, ii) Propagation delay, iii) Fan-in, iv) fan-out. f) What is the programmable table of PLA? How is the capacity of a PLA specified?	5x4=20
Q 3.	Answer any two parts of the following. a) Design a 4-bit binary up down ripple counter, also show its clock diagram. b) Simplify the Boolean function F (A, B, C, D): ∑ (1, 3, 7, 11, 12, 13) which has the don't care condition d (A, B, C, D): ∑ (0, 2, 5, 9) and then express the simplified function in sum-of-minterms forrn. c) What is a TTL NAND gate? Draw the circuit diagram of a standard TTL NAND gate.	10x2= 20
Q 4.	Answer any two parts of the following. a) Explain the truth table of the SR, JK, D & T flip-flops. b) Solve the logic function given below, using Quine McClusky minimization technique and realize simplified expression using universal gates. F (A, B, C, D) = ∑ (0, 1, 3, 7, 8, 9,11, 15) c) What is dataflow modeling in VHDL? Explain the behavioral modeling in VHDL? What are the advantages of using dataflow modeling?	10x2= 20
Q 5.	Answer any two parts of the following. a) Explain different logic gates families in digital circuits. Write a short note on universal gate. b) Solve the following Boolean functions by using K-Map: F(a, b, c, d) = ∑ (0, 1, 4, 5, 6, 8, 9, 10, 12, 13, 14) c) What is an FPGA? Describe the basic architecture of an FPGA. How is an FPGA programmed?	10x2= 20

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